

TEMU
PowerPC Target Manual

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Table 1. Record of Changes

Rev	Date	Author	Note
1.0	2018-11-28	MH	Initial version.

1. Introduction

The PowerPC target in TEMU comes with support for the 32 bit PowerPC architecture. It currently implements the PPC750 CPU model. The target is in beta-state at time of writing.

2. Variants

2.1. PowerPC 750

The PPC 750 is a 32 bit PowerPC without AltiVec support.

3. Configuration

3.1. Arguments

3.2. Properties

3.2.1. Interface References

memaccess

The interface reference to an object reacting to the emulator core's memory accesses (whenever there is an ATC miss). This should normally refer to a memory space object or the MMU interface. Set this to `memspace:MemAccessIface` in case the CPU lacks an MMU or to `cpu:MmuMemAccessIface` in-case the CPU has an MMU. That is, in the case of an MMU, the iface reference refers to the object itself.

memory

The interface reference to an object handling memory block read and writes, this should normally refer to a memory space object.

irqctrl

The interface reference to an object implementing the IrqControl interface. This can be used to connect external interrupt controllers which need to have interrupts acknowledged.

3.2.2. Other Properties

freq

Clock frequency in Hz. Defaults to `50000000 = 50 MHz`.

cpuid

CPU id for multiprocessor configurations, defaults to 0.

3.3. Interfaces

The SPARCV8 emulator cores implement the following interfaces:

CpuIface

The common CPU interface. This contain functions like run and register access functions.

PowerPCIface

Standard PowerPC interface. Exposes convenient functions for accessing SPRs.

IrqIface

The interrupt controller interface for raising interrupts on the processor.

InvalidMemAccessIface

Interface invoked on invalid memory accesses. This contain functions that will longjmp to the CPU trap handling logic. The interface can only be invoked from code invoked by the CPU core in one way or the other. Do not call the functions in this interface directly!

EventIface

Interface for posting timed events on the CPU core's event queue. Usually a reference to this event is installed in connected device models.

MemoryIface

Proxy interface which forwards to the memory space object.

4. Limitations

Current known limitations of the PowerPC target include:

- No static timing model is defined at this moment. That means that one instruction take one cycle to finish.
- The built-in assemblers and disassemblers are not working at this have problems with split field instructions (e.g. SPR IDs).
- Cache control interfaces are not implemented or supported, this can be addressed if needed.
- AltiVec instructions are not implemented at this moment. These can be added if such a PowerPC model is requested.
- MMU model is not yet validated against hardware.