

TEMU
GRPCI2 Model

Mattias Holm

Version 1.0, 2019-12-12

Table of Contents

| | |
|----------------------------------|---|
| 1. Introduction | 1 |
| 2. Loading the Plugin | 1 |
| 3. Configuration | 1 |
| 4. Attributes | 1 |
| 4.1. Properties | 1 |
| 4.2. Interfaces | 1 |
| 4.3. Ports | 2 |
| 5. Registers | 2 |
| 5.1. Register Bank default | 2 |
| 6. Limitations | 2 |

1. Introduction

The GRPCI2 model is available in the GrPci2 plugin.

2. Loading the Plugin

```
import GrPci2
```

3. Configuration

4. Attributes

4.1. Properties

| Name | Type | Description |
|-------------------|-------------------------|--|
| AHB2PCI | uint32_t | AHB to PCI mapping for PCI I/O |
| AHBM2PCI | [16 x uint32_t] | DMA channel active |
| BCIM | uint32_t | PCI master prefetch burst limit |
| CTRL | uint32_t | Control register |
| DMABASE | uint32_t | DMA descriptor base address |
| DMACHAN | uint32_t | DMA channel active |
| DMACTRL | uint32_t | GRPCI2 DMA control and status register |
| PCI2AHB | [6 x uint32_t] | DMA channel active |
| STATCAP | uint32_t | Status and Capability register |
| ioMem | iref / MemorySpaceIface | PCI i/o space object |
| irqCtrl | iref / IrqCtrlIface | Upward interrupt controller (i.e. on AMBA bus) |
| object.timeSource | object | Time source object (a cpu or machine object) |
| pciMem | iref / MemorySpaceIface | PCI memory space object |

4.2. Interfaces

| Name | Type | Description |
|----------|----------|-------------------|
| ApbIface | ApbIface | APB P&P interface |

| Name | Type | Description |
|-------------------|----------------------|-------------------------------------|
| ConfigAccessIface | MemAccessIface | PCI config access interface. |
| IrqIface | IrqCtrlIface | PCI IRQ interface |
| MemAccessIface | MemAccessIface | Memory access interface (registers) |
| PCIBridgeIface | temu::PCIBridgeIface | PCI bridge interface. |

4.3. Ports

| Prop | Iface | Description |
|------|-------|-------------|
| - | - | - |

5. Registers



Register support is currently experimental!

5.1. Register Bank default

6. Limitations

- The device currently only supports one AHB master. Since most systems only have one (e.g. an AHB2AHB bridge), this limitation should not be a major issue.