T-EMU: GRLIB IrqMp Device Model Manual

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Record of Changes

Author	Description	Rev	Date
Mattias Holm	Auto gen tables	1.1	2016-05-12
Mattias Holm	Initial Version	1.0	2015-07-31

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1. Introduction

The IrqMP is part of the GRLIB device library from Gaisler. It is a multiprocessor capable interrupt controller.

The controller supports among things the routing of interrupts to different processor cores, and also broadcasted interrupts.

2. Configuration

config.nCpu	Number of processors supported.
config.enExtIrq	Enable extended IRQs.
pnp.config	Plug and play configuration word for APB plug-and-play.
cpu	Up to 16 CPUs supported. IfaceRef property should be connected to the different CPUs.

3. Attributes

3.1. Properties

Name	Type	Description
broadcast	uint32_t	
config.enExtIrq	uint8_t	
config.logInterrupts	uint8_t	

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Name	Type	Description
config.nCpu	uint8_t	
config.traceReads	uint8_t	
config.traceWrites	uint8_t	
cpu	[16 x iref]	
extIntAck	[16 x uint32_t]	
force	[16 x uint32_t]	
irqClear	uint32_t	
irqCtrl	[16 x iref]	
irqForce0	uint32_t	
irqLevel	uint32_t	
irqPending	uint32_t	
mask	[16 x uint32_t]	
mpStatus	uint32_t	
object.timeSource	object	Time source object (a cpu or machine object)
pnp.bar	uint32_t	
pnp.config	uint32_t	

3.2. Interfaces

Name	Type	Description
ApbIface	ApbIface	
DeviceIface	DeviceIface	
IrqClientIface	IrqClientIface	uptree interrupt handlers (e.g. CPUs)
IrqIface	IrqCtrlIface	
MemAccessIface	MemAccessIface	
ResetIface	ResetIface	

3.3. Ports

Prop	Iface	Description
irqCtrl	IrqClientIface	irq port

4. Limitations

The following deviations from real hardware are known to exist with this model:

- Broadcasted interrupts are broadcasted at the current time to all CPUs, if it was triggered by a non-synchronised event, the interrupt is raised at different times on the different cores. Depending on the IRQ frequency and the configured quanta length, this may result in problems.

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