

T-EMU: GRLIB GPTIMER Device Model Manual



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Table of Contents

1. Introduction	2
2. Configuration	2
2.1. Separate Interrupts	2
2.2. Interrupt Index	2
2.3. Number of Timers	2
2.4. Clear IRQ on Set	2
3. Limitations	3

1. Introduction

The GPTIMER is part of the GRLIB device library from Gaisler. The timer runs using synchronised events in order to ensure that would a timer tick be broadcasted by the interrupt controller, then the IRQ should be taken at roughly the same time.

2. Configuration

2.1. Separate Interrupts

Set the "config.separateInterrupts" property to non-zero.

2.2. Interrupt Index

The interrupt number can be set by configuring the "pnp.config" property. The lower 5 bits of the property is used for this.

2.3. Number of Timers

Set the "config.numTimers" property. By default this value is 4 to be compatible with the UT699.

2.4. Clear IRQ on Set

Set the "config.clearIrqOnSet" property changes the behaviour of bit 4 in the timer control registers. ClearOnSet can be non-zero (the default), in that case writing a 1 to the bit will clear bit 4 (i.e. it will read out as 0), if clearOnSet is zero, the bit is cleared if bit 4 is 0 in the written word.

The reason for this are ambiguities in the LEON3 and UT699 manuals.

3. Limitations

The following deviations from real hardware are known to exist with this model:

- The Disable Timer Freeze bit is always 1 and cannot be configured.
- The Debug Halt bit for each timer is always 0 and cannot be altered.
- Chained timers are not supported at the moment.
- The last timer does not work as a watchdog.
- As the timer utilise synchronised events, the minimum time for a timer expiration on a multi-core CPU would be equal to the time-quanta that the machine has been configured with.